Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

controlling a sense array of a memory to ~~sensing~~ sense a first word group from a first address of [[a]] the memory while controlling the sense array to ~~sensing~~ sense a second word group from a second address of the memory, wherein the second address is at a non-contiguous initial address with respect to the first address; and

controlling the sense array to sense a third word group from a third address of the memory, wherein the third word group corresponds to the width of the first and second word groups combined.

Claim 2 (currently amended): The method of claim 1, wherein the first word group is half as wide as a sense width of [[a]] the sense array of the memory.

Claim 3 (original): The method of claim 1, further comprising synchronously reading the first word group and the second word group from the memory.

Claim 4 (original): The method of claim 1, further comprising separating a request for the first word group from a request for the second word group by a predetermined number of clock cycles.

Claim 5 (original): The method of claim 4, wherein the predetermined number equals four.

Claim 6 (original): The method of claim 1, wherein the first word group comprises four double words.

Claim 7 (original): The method of claim 1, further comprising using a first latch to latch the first address and a second latch to latch the second address.

Claim 8 (currently amended): A method comprising:

sensing a first burst length of data at a first initial address, the first burst length of data equal to half of a sense width of a plurality of sense amplifiers of a memory; and

sensing a second burst length of data at a second initial address that is non-contiguous to the first initial address, the second burst length of data equal to the half of the sense width, at least partially during a latency before reading the first burst length of data.

Claim 9 (cancel)

Claim 10 (original): The method of claim 8, wherein sensing the first burst length of data comprises sensing four double words of data.

Claim 11 (original): The method of claim 8, further comprising sensing a third burst length of data equal to the half of the sense width after sensing the first burst length.

Claims 12 – 17 (cancel)

Claim 18 (currently amended): A system comprising:

a memory having a sense array to overlappingly sense a first word group from a first initial address and a second word group from a second initial address, or to sense a third word group from a third initial address, wherein the third word group is twice as wide as the first word group; and

a dipole antenna coupled to the memory.

Claim 19 (currently amended): The system of claim 18, further comprising a first latency counter to track a latency associated with a read operation of the first word group, and a second latency counter to track a latency associated with a read operation of the second word group.

Claim 20 (currently amended): The system of claim 18, wherein the sense array has a width twice that of the first word group, and equal to that of the third word group.

Claim 21 (original): The system of claim 18, further comprising a first output buffer coupled to a first portion of the sense array, the first portion corresponding to a width of the first word group.

Claim 22 (currently amended): An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

control a sense array of a memory to sense a first word group from a first address of [[a]] the memory while controlling the sense array to sense a second word group ~~is sensed~~ from a second address of the memory, wherein the second address is at a non-contiguous initial address with respect to the first address; and

control the sense array to sense a third word group from a third address of the memory, wherein the third word group corresponds to the width of the first and second word groups combined.

Claim 23 (original): The article of claim 22, further comprising instructions that if executed enable the system to synchronously read the first word group and the second word group from the memory.

Claim 24 (original): The article of claim 22, further comprising instructions that if executed enable the system to separate a request for the first word group from a request for the second word group by a predetermined number of clock cycles.

Claim 25 (cancel)

Claim 26 (new): The system of claim 18, further comprising a controller to configure the sense array to sense the first and second word groups or the third word group.

Claim 27 (new): An apparatus comprising:

a memory array to store data;

a sense array coupled to the memory array to sense data from the memory array, wherein the sense array is configured to overlappingly sense first data groups from a plurality of non-contiguous initial addresses, each of the first data groups half as wide as a sense width of the sense array, or sense a second data group from a third initial address, wherein the second data group corresponds to the sense width of the sense array; and

a controller coupled to the sense array to configure the sense array based on a read request for data in the memory array.

Claim 28 (new): The apparatus of claim 27, further comprising an output multiplexer coupled to the sense array.

Claim 29 (new): The apparatus of claim 28, wherein the controller is to control the output multiplexer to output a first one of the first data groups sensed from a first one of the plurality of non-contiguous initial addresses while the sense array is to sense a second one of the first data groups from a second one of the plurality of non-contiguous initial addresses.

Claim 30 (new): The apparatus of claim 27, further comprising a first latch to latch a first one of the plurality of non-contiguous initial addresses and a second latch to latch a second one of the plurality of non-contiguous initial addresses.

Claim 31 (new): The apparatus of claim 27, further comprising a first latency counter to track a latency associated with a read operation of a first one of the first data groups, and a second latency counter to track a latency associated with a read operation of a second one of the first data groups.

Claim 31 (new): The apparatus of claim 27, wherein the memory comprises a nonvolatile memory.

Claim 32 (new): The method of claim 8, further comprising sensing a thirst burst length of data at a third initial address, wherein the third burst length of data is equal to the sense width of the plurality of sense amplifiers.